A 69 GHz MONOLITHIC FET OSCILLATOR*

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ABSTRACT

A monolithic oscillator was fabricated using conventional planar FET technology. The active device used was a 0.35x60 micron FET fabricated on an active layer formed by ion implantation into an undoped VPE buffer layer. Frequency stability is achieved using either an on-chip microstrip resonant circuit or by adding a 30 mil diameter dielectric resonator directly onto the 50 mil square GaAs chip. With no external tuning the oscillator delivered 0.45 milliwatts at 64 GHz. By using an external E-H waveguide tuner, 0.7 milliwatts of power at 65.7 GHz was achieved. The oscillator was tunable from 55 to 75 GHz by adjusting the source-gate tuning inductor and the drain tuning.

INTRODUCTION

Monolithic GaAs integrated circuits have been demonstrated for a wide variety of applications at frequencies from DC to 20 GHz. At millimeter wave frequencies, however, monolithic IC applications have been limited primarily to diode based mixers due to a lack of available active devices. Recently, quarter micron gate length discrete FETs have demonstrated themselves to be useful, active devices at frequencies up to 60 GHz and monolithic FET based amplifiers and oscillators are becoming attractive components for millimeter wave systems. This paper describes the development of a simple V-band monolithic oscillator using a planar quarter micron FET as its active device.

DEVICE DESCRIPTION

The oscillator design was based on the properties of a planar GaAs FET with a 0.25x60 micron gate reported previously.[1] The device structure consists of a pair of 0.25x30 micron gate fingers fabricated using a direct write E-beam lithography system with the gate offset towards the source in the channel to reduce the source resistance. The active layers were formed using both VPE and ion implantation. The discrete devices were DC characterized and their S-parameters were measured from 2-18 GHz using a conventional network analyzer. This data was used to construct a lumped device equivalent circuit shown in Figure 1. This model was then used to project the performance of the device up to 100 GHz. This is, admittedly, an approximation but it was felt that this would provide better design data than trying to measure S-parameters directly at 60-70 GHz. Figure 2 shows a plot of the calculated maximum available gain of FETs from four separate wafers plotted versus frequency and based on measured 2-18 GHz S-parameters. The devices show an f_{max} of 88 to 105 GHz and should make useful amplifiers up to 60 GHz and oscillators to 80 GHz. This calculated data is roughly confirmed by the fact that 60 GHz hybrid amplifiers fabricated from these devices provide 6-7 dB gain.[1]

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OSCILLATOR DESIGN

Unlike two-terminal Gunn or IMPATT diodes, typically used to fabricate millimeter wave oscillators, an FET does not possess an inherent negative resistance and external feedback elements must be provided to the device to obtain oscillation.

Microwave oscillators generally can be reduced to the basic Colpitts configuration shown in Figure 3a. Here, the frequency of oscillation is set by the resonant frequency of the inductance-capacitance loop, with the FET acting as the active source sustaining the loop current. Actually, the capacitances (C_1 and C_2 in Figure 3) often are internal device interelectrode capacitances which are simply incorporated into the oscillator circuit. Any of the three device terminals can be connected to ground. The circuit still can be analyzed as a Colpitts oscillator. Selection of the terminal to connect to ground should be based on ease of coupling to the load, effects of parasitics and thermal considerations.

Two popular oscillator configurations, the common gate and the common drain, also are shown in Figure 3. In

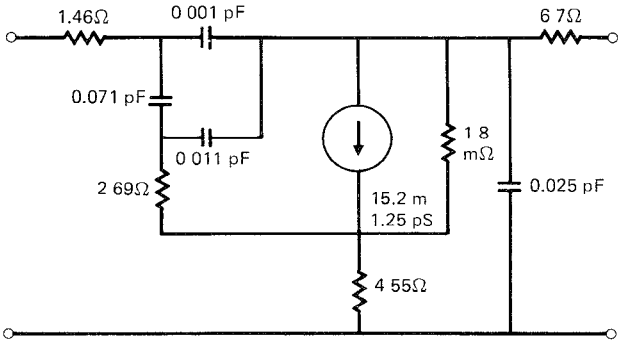

Fig. 1 Discrete FET equivalent circuit.

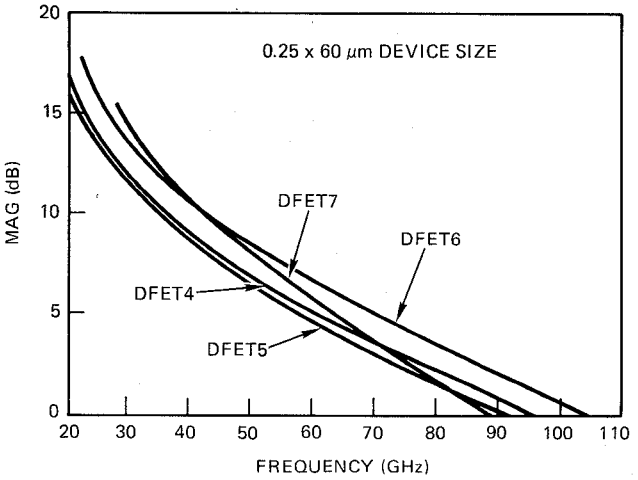

Fig. 2 Calculated maximum available gain vs frequency.

both configurations, C_1 usually is the internal gate-to-source interelectrode capacitance. Often, C_2 also is internal. In the common gate and common drain configurations, the load usually is coupled to the oscillator at the drain and source terminals, respectively. To oscillate, the Colpitts oscillator simply requires a net inductive reactance connected between the gate and drain.

Using the equivalent circuit of DFET 6 and calculating the input impedance looking into the drain of a grounded gate FET with an inductance in the source lead, we form a Colpitts oscillator and obtain impedance versus frequency as shown in Figure 4. A small signal negative resistance is shown from 61 to more than 100 GHz, but its magnitude at 90 is only -6 ohms with a Q of 9. A simple series inductance can be used to match the drain circuit and a microstrip resonator or a dielectric resonator as shown in Figure 5 can be used to stabilize the output. Abe et al[2] have described the technique of using

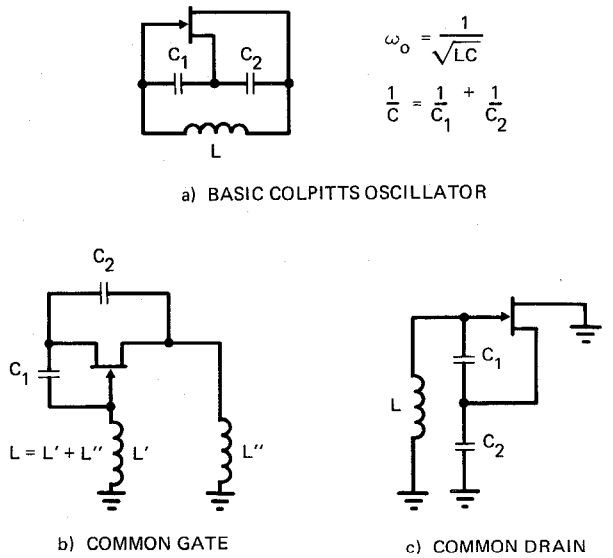

Fig. 3 FET oscillator circuits.

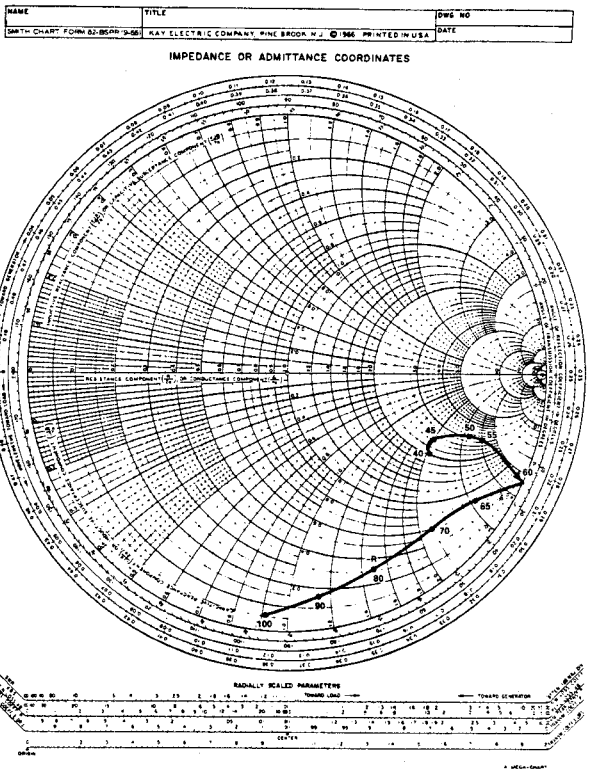

Fig. 4 Calculated input impedance.

a dielectric resonator between drain and load to stabilize an FET oscillator. Basically, the dielectric puck is coupled to the microstrip transmission line forming a single pole bandstop filter. This is placed approximately a half wavelength from the active device. The oscillator can be then mechanically tuned by optimizing both the distance from the device and the separation from the microstrip line. This violates some of the basic principles of monolithic IC's in that we are adding a chip component and are physically tuning the circuit, but it provides twice the Q of a microstrip cavity and allows us to compensate for design uncertainties.

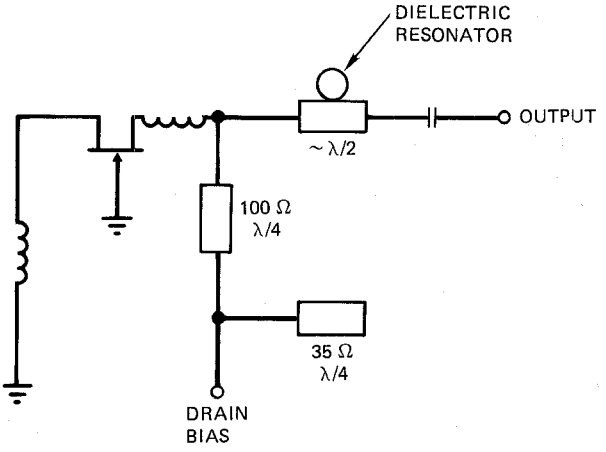

Fig. 5 Equivalent circuit of dielectric resonated oscillator.

OSCILLATOR FABRICATION

The monolithic oscillator is shown in Figure 6. It consists of a 0.35x60 μm single strip gate. The gate is directly grounded, and the source is grounded through a pair of high impedance microstrip transmission lines which can be adjusted easily using a wire bonder to vary the length. A simple, low-Q matching circuit is used to achieve oscillation over a range of frequencies with a minimum of tuning on chip. The chip size, 50x50x4 mils, allows additon of an on-chip dielectric resonator.

The high reactance at the gate terminal mandates that a high impedance inductor be used for matching, to avoid seriously degrading the small negative resistance. Conventional microstrip on 100 μm GaAs is limited by photolithographic and loss considerations to a maximum impedance of about 85 ohms. This impedance is inadequate for the oscillator circuit. For this application, a new, high-impedance transmission line was developed using a 12 micron high airbridge. The large airgap reduces the capacitance to ground by a factor of two and can, therefore, increase the impedance of the structure by as much as 40 percent.

The active device and the end of the high airbridge are shown in Figure 7.

The oscillators were fabricated on an active layer formed by ion implanting singly charged silicon at an energy of 100 KeV for a total dose of 6E12 atoms/cm^2 into a VPE undoped buffer layer. Isolation was accomplished by mesa etching through the active layer. The circuits were processed using optical masks generated on an E-beam pattern generator, and the gates were direct written on the same machine. The gate uses a Ti-Pt-Au metallization system and was designed to be 0.25 μm long but slight overexposure yielded 0.35 μm gates.

The wafer contained 161 devices, of which 53 or 33 percent were visual and dc good. The FET has an

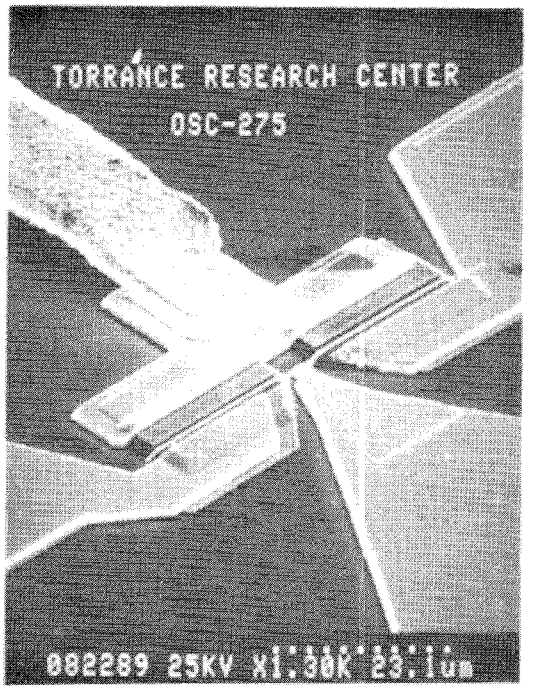

Fig. 7 Details of FET.

average I_{DSS} of 17.7 mA, with a standard deviation of 15 percent. The pinch-off voltage is 3 V, and the transfer conductance (gm) at zero bias is 8 ms. This gm is somewhat lower than seen on devices from wafers DFET 4 through 7 on which the design was based.

The oscillators were tested by coupling them to a waveguide, as shown in Figure 8. A microstrip probe on a 7-mil-thick quartz substrate protrudes into the broad wall

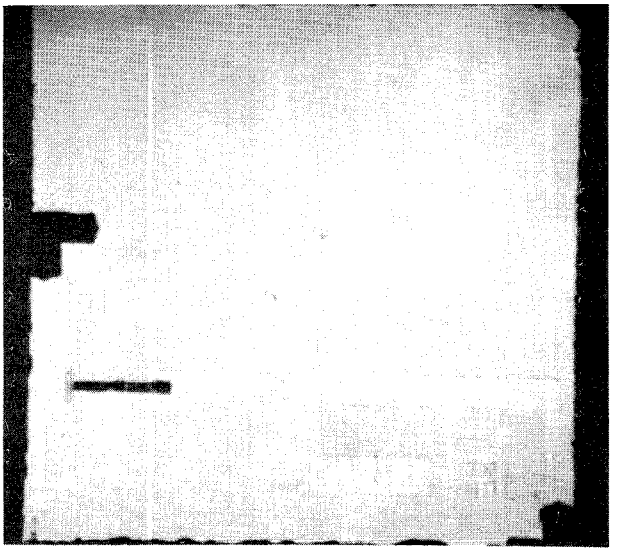

Fig. 6 Monolithic oscillator.

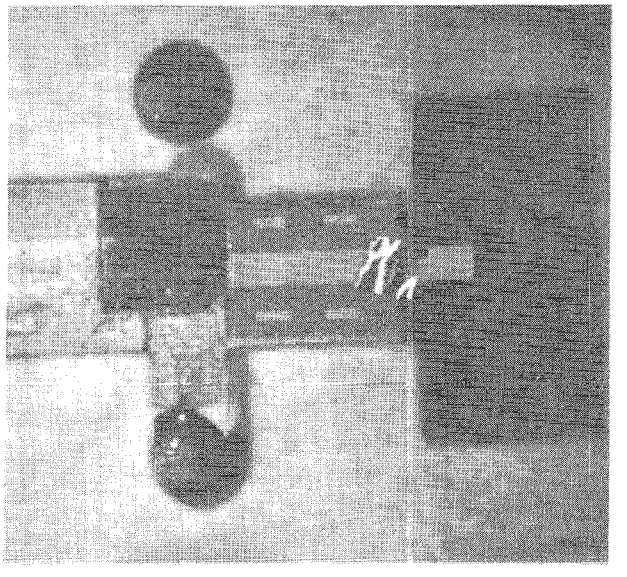

Fig. 8 Oscillator coupled to V band waveguide.

of the V-band waveguide, forming an E-plane probe. A pair of these probes including an additional 0.3 inch of microstrip line has approximately 1 dB of insertion loss at 60 GHz. A low impedance transmission line formed on K-100 material forms an off-chip bias decoupling network. The complete waveguide test fixture is shown in Figure 9.

With no external tuning the oscillator delivered 0.45 mW at 64 GHz. An external E-H tuner and gold foil tuning on the microstrip transmission lines were used to optimize performance. Figure 10 shows the optimum power output versus drain voltage. We achieved 0.7 milliwatt at 65.7 GHz with 4 volts on the drain and 1 percent efficiency. As shown in the Figure, dropping the drain voltage did reduce the power output but varied the output frequency less than 50 MHz. The oscillator frequency was continuously adjustable up to 75 GHz, with the output power tapering off to zero.

As mentioned earlier, it is possible to adjust the negative resistance of the oscillator by tuning the gate-source inductance and retuning the drain circuit. Figure 11 shows the result of tuning this inductor from 0.06 to 0.14 nH by means of bonding straps across the source transmission lines. A maximum frequency of 78.2 GHz was obtained with 0.2 mW of power delivered. This result was obtained with the aid of an EH tuner on the output.

To improve the stability of the oscillator we machined dielectric pucks, fabricated from Barium tetratitanate which has a dielectric constant of 37. The resonators were tested on a microstrip on 7 mil quartz test fixture shown in Figure 12. An unloaded Q of 247 was obtained at 76 GHz. The oscillators have been measured with several sizes of resonators and preliminary

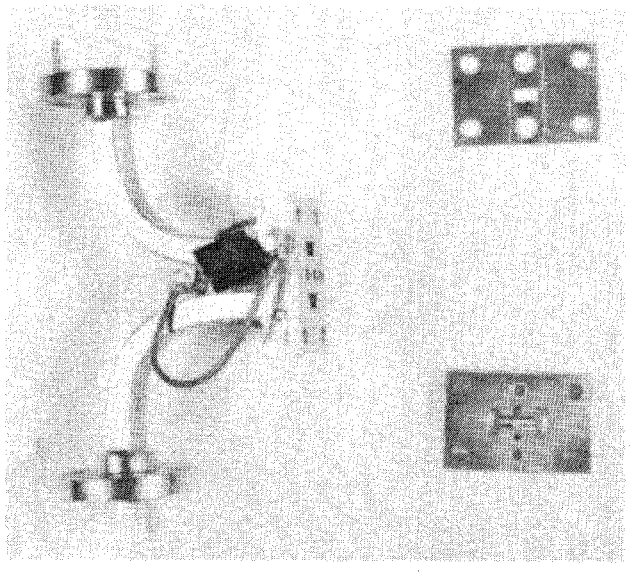

Fig. 9 Waveguide test hardware.

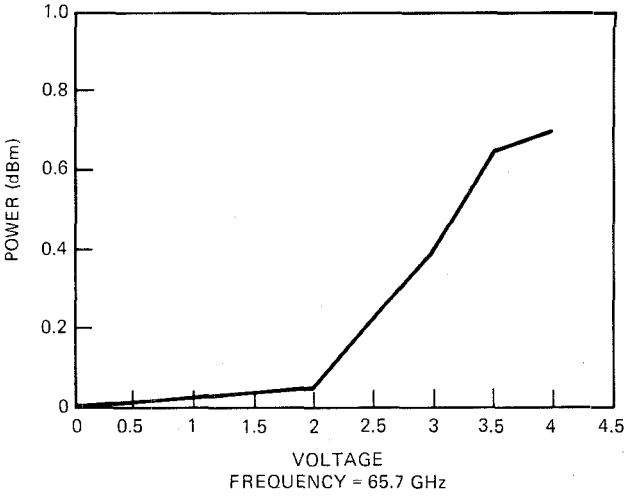

Fig. 10 Power versus voltage for the monolithic oscillator.

results show 1 to 1.2 mW of power delivered at 57.2 GHz and 0.5 mW at 67.9 GHz.

SUMMARY

A monolithic FET oscillator has been developed with 0.5-1.0 mW available from 60-70 GHz with an efficiency of 1 percent or less. The oscillators can be stabilized using conventional dielectric cavities but are difficult to work with due to the small size. Microstrip cavities are somewhat easier to work with, but have unloaded Q's of half that available from dielectric pucks. The conversion efficiency is somewhat lower than expected and work is continuing.

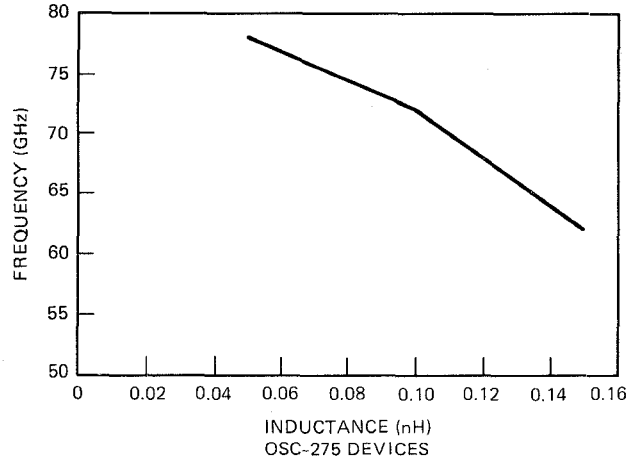

Fig. 11 Maximum frequency of oscillation as a function of G-S inductance.

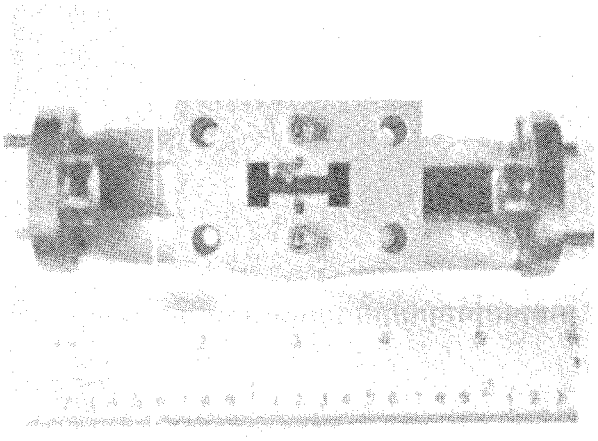

Fig. 12 Resonator test fixture.

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